MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

EEE3196 – INTEGRATED VLSI SYSTEMS

(All sections / Groups)

7 MARCH 2016
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 7 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\Phi T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\,R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) AVoltage Transfer Characteristics (VTC) graph is shown in Figure Q1(a).

(i) Redraw the VTC graph and label the critical voltages, V_{IL}, V_{IH} and V_M on the graph.

(ii) In the VTC graph, state the operating modes range for both PMOS and NMOS on the graph.

[5 marks]

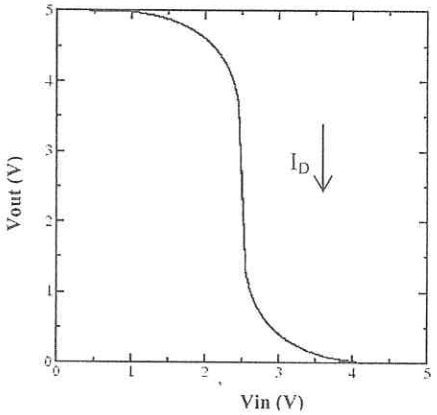

Figure Q1 (a)

(b) Given a CMOS inverter with the following parameters:
$k'_n = 50\ \mu A/V^2$, $k'_p = 20\ \mu A/V^2$, $V_{Tn} = |V_{Tp}| = 1$ V, $V_{DD} = 3.3$ V, $V_{GS} = 3.3$ V, $(W/L)n = 2$, $(W/L)p = 5$ and $C_L = 50$ fF.

(i) Calculate the current (I_d) of the NMOS transistor when it is operating at:
- saturation region ($V_{out} = 3.3$ V), and
- linear region ($V_{out} = 1.7$ V).

[4 marks]

(ii) Using the average current (I_{avg}) method, find the high-to-low propagation delay (t_{PHL}). [4 marks]

(iii) Using the average on-resistance (R_{on}) method, find the high-to-low propagation delay (t_{PHL}). [4 marks]

(iv) Compare the answers for two different methods in Q1(b)(ii) and Q1(b)(iii) above and comment.

[2 marks]

(v) Calculate the power-delay-product (PDP) of the CMOS inverter, assuming that the frequency, f = 10 kHz and the static current is equivalent to 50 μA.

[6 marks]

Continued...

Question 2

(a) Consider a metal1 aluminium interconnect wire line overlapping an active area as shown in Figure Q2 below. Assume sheet resistance of the metal1 wire is given as 30 Ω/square and the typical interwire capacitance values are:

Area capacitance = 0.041 ± 0.004 fF/μm^2

Fringing capacitance = 0.047 ± 0.004 fF/μm

(i) Calculate the total resistance with this line.

(ii) Calculate the total capacitance associated with this line.

(iii) Based on part (i), the total capacitance is due to parallel plate capacitance and fringing capacitance. Evaluate these two capacitances and comment.

[7 + 7 + 2 marks]

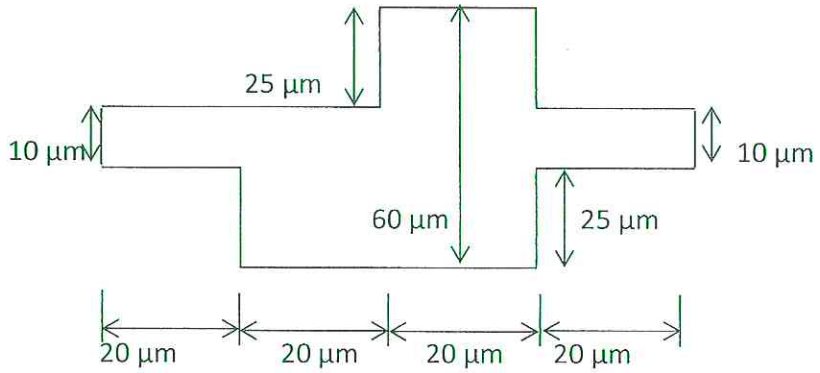

Figure Q2

(b) Crosstalk in electronic circuit is an undesired phenomena which usually caused by undesired effect from another circuit.

(i) Explain how crosstalk can happen in digital integrated circuit.

(ii) Recommend TWO ways to reduce the capacitive crosstalk.

[6 marks]

(c) Packaging plays an important role in component's operation and performance. State THREE requirements for a good IC packaging.

[3 marks]

Continued...

Question 3

(a) Given the following function:

$$F = \overline{A \cdot (B + \bar{C})}$$

(i) Design and sketch the circuit for this function F using conventional static CMOS transistors.

(ii) Modify the design in part (i) using following methods:

a. pseudo NMOS

b. dynamic logic

(iii) Based on the designs in part (ii), distinguish and elaborate on the difference between pseudo NMOS and dynamic logic from circuit structure point of view.

[6+6+4 marks]

(b) In combinational logic designs, normally capacitance dominates the parasitic in the circuit. Describe TWO design techniques that would help reduce the capacitance parasitic.

[4 marks]

(c) Figure Q3 shows the output results for cascading two dynamic gates. The output *Out2* shows a reduced value when the *Clk* is triggered high.

Suggest modification on the circuit to solve this dynamic logic cascading issue. Describe the operation for the suggested circuit as well.

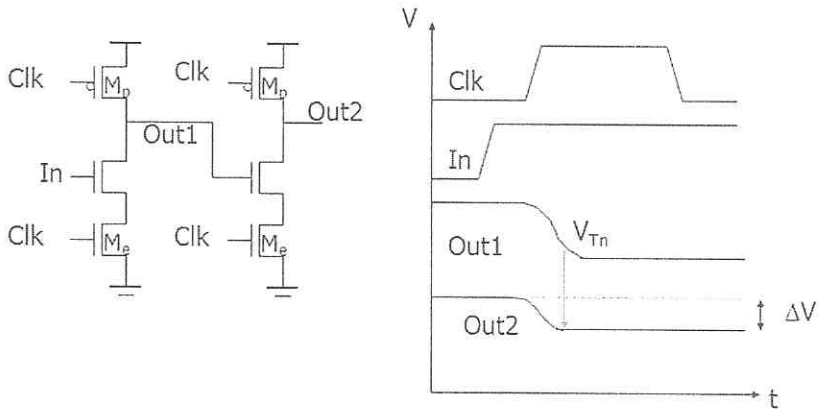

Figure Q3

[5 marks]

Continued...

Question 4

(a) Given an 8-bit ripple carry adder (RCA) with its t_{carry} = 400 ps and t_{sum} = 500 ps.
(i) Find the worst case delay t_{adder}.
(ii) Give an example of input values that will trigger this worst case delay.
(iii) Based on part (i) and (ii), comment on the optimization goal needed to have a fastest RCA.

[3+2+4 marks]

(b) The structure of a barrel shifter is shown in Figure Q5(a).
(i) Describe briefly the barrel shifter operation.
(ii) Explain THREE differences between the barrel shifter and a logarithmic shifter.

[4+6 marks]

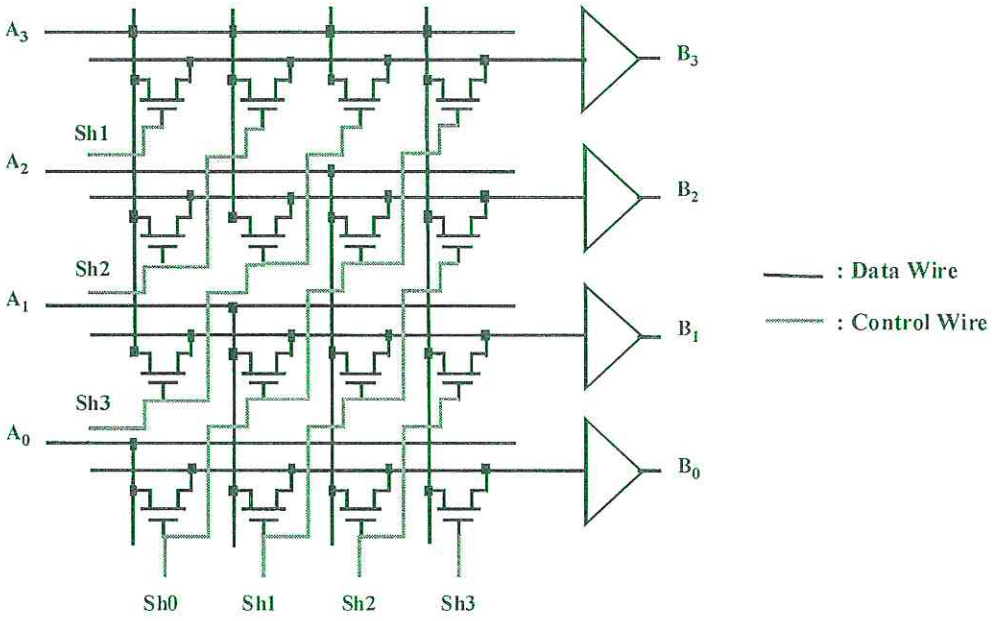

Figure Q5(b)

Continued...

(c) Refer to Figure Q5(c) below,

(i) Comment on the Non-Volatile Memory Trend especially on NAND Flash and RRAM.

(ii) State two other types of Non-Volatile Memory.

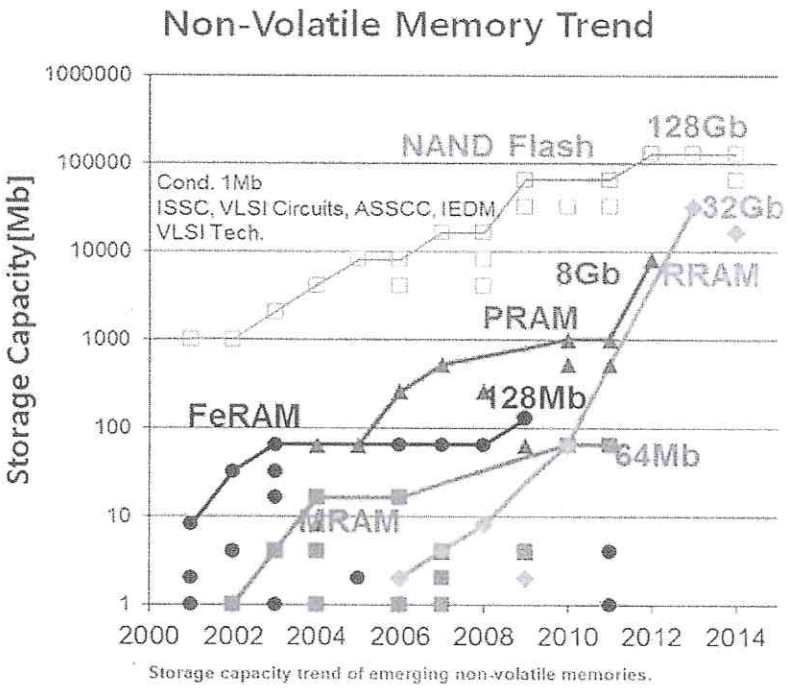

Figure Q5(c)

[6 marks]

End of Paper